		O-1449 (modified) nts and Publications	ATTY. DKT. NO. 5181-37601 APPLICANT: Bodo K. Parady		SEI	SERIAL NO 10/044,487 GROUP: 2183 Fig. 10/0 6 2007		
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			J.S. PATENT	T DOCUMENTS		P. S. C.	CELLA	
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		OTHER ART (I	ncluding Auth	or, Title, Date, Pertinent Pa	ges, Etc.)			
450	Al	"Load Latency Tolerance In Dynamically Scheduled Processors"; IEEE 1998; Srinivasan & Lebeck; Duke University, Department of Computer Science; Durham, North Carolina						
077}	A2	"Discrete Last-Address Predictor"; Morancho, Llaberia, & Olive; Universitat Politecnica de Catalunya, Department d'Arquitectura de Computadores; Barcelona (Spain)						
977	A3	"Understanding the Differences Between Value Prediction and Instruction Reuse"; Sodani & Sohi; University of Wisconsin-Madison, Computer Sciences Department; Madison, Wisconsin						
9571	A4	"The Predictability of Data Values"; Sazeides & Smith; University of Wisconsin-Madison, Department of Electrical and Computer Engineering; Madison, Wisconsin						
400	A5	"Speculative Execution via Address Prediction and Data Prefetching"; Gonzalez & Gonzalez; Universitat Politecnica de Catalunya, Department d'Arquitectura de Computadors; Barcelona (Spain)						

EXAMINER: Dand & Thinn

DATE CONSIDERED:

8-10-04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.